

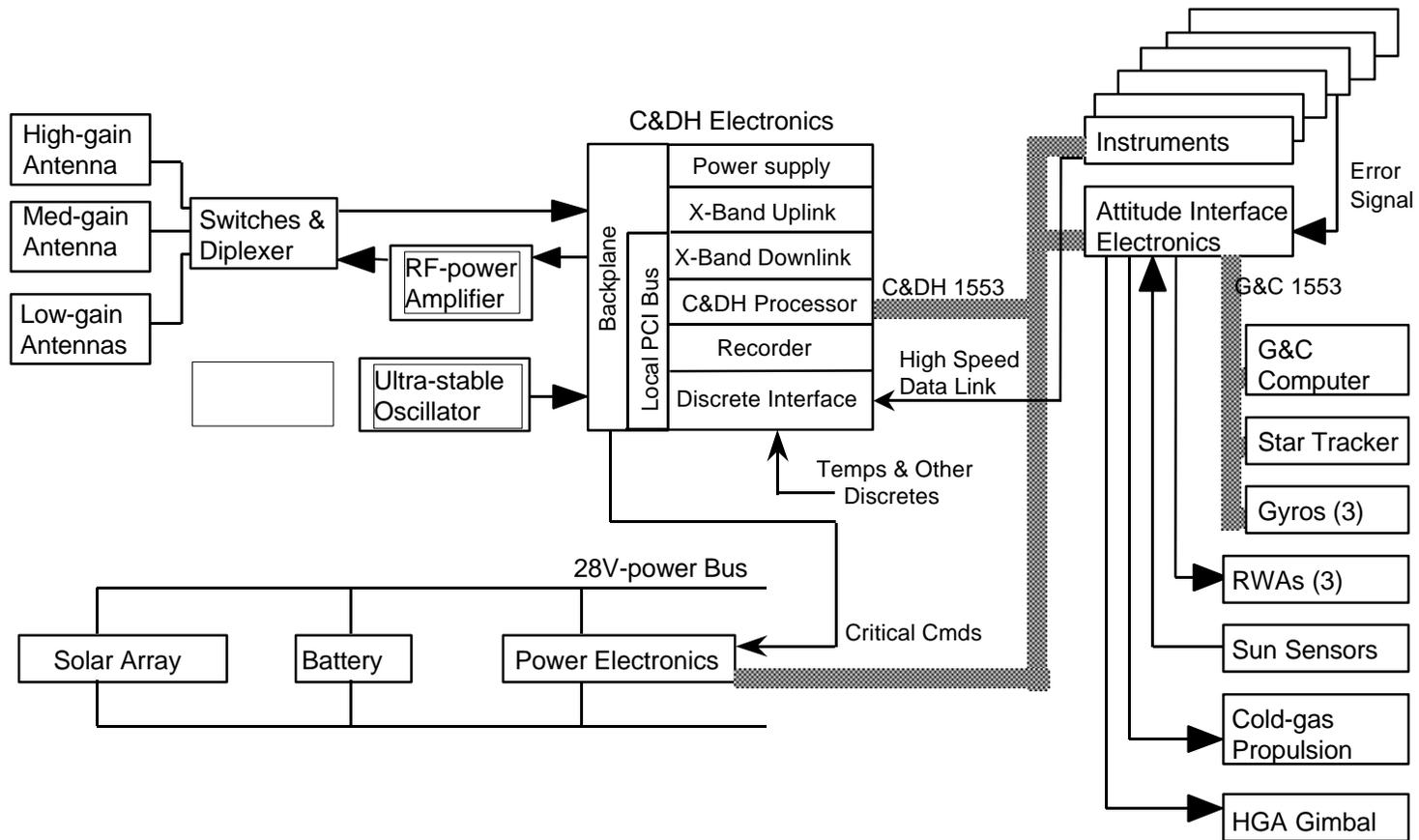
STEREO
Command & Data Handling System
Description

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C&DH REQUIREMENTS

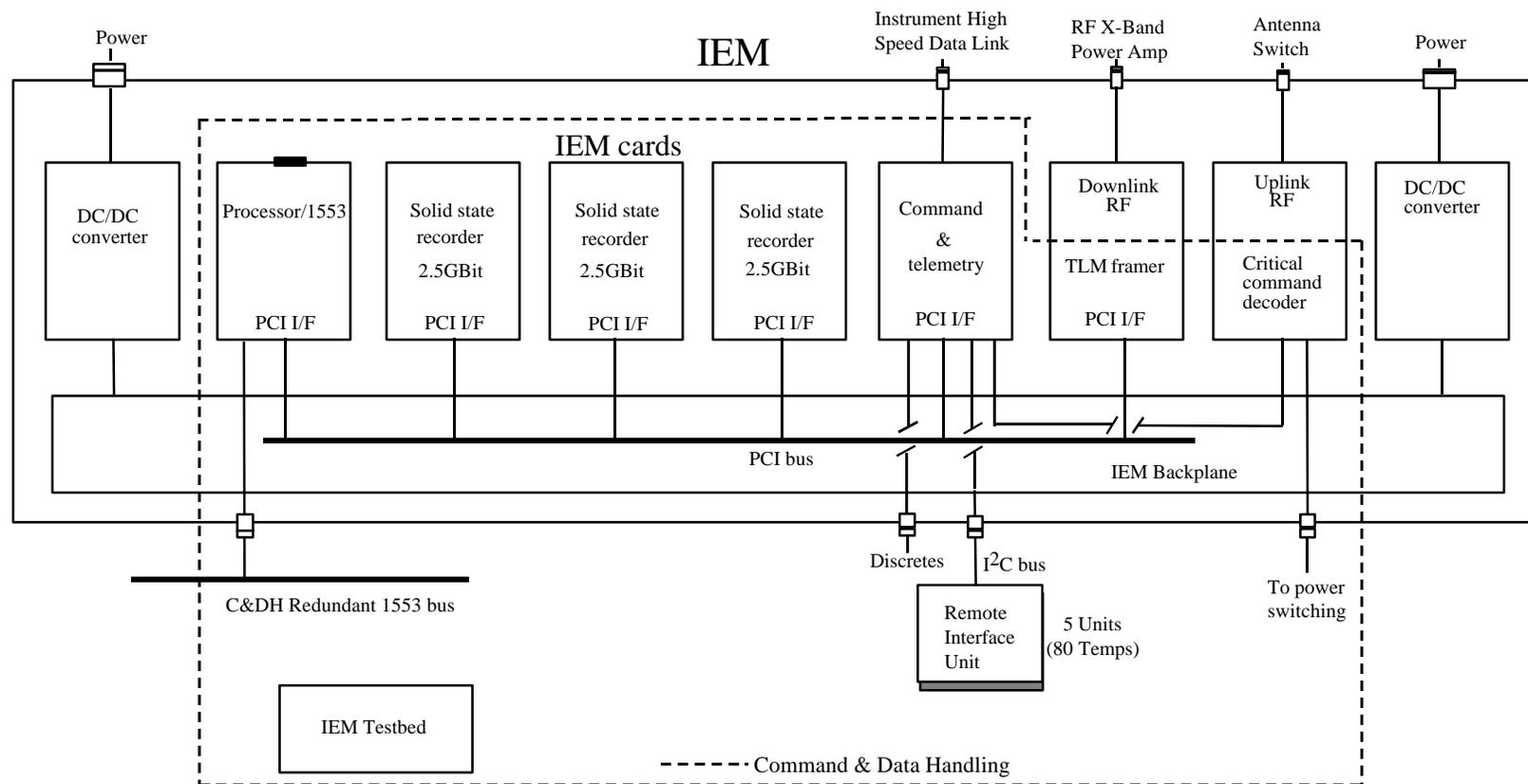
- Uplink and stored command management
- Telemetry data collection and processing
- Mass storage of science and engineering data
- Autonomous fault protection
- Subsystem intercommunication
- UT maintenance & distribution

Spacecraft Block Diagram

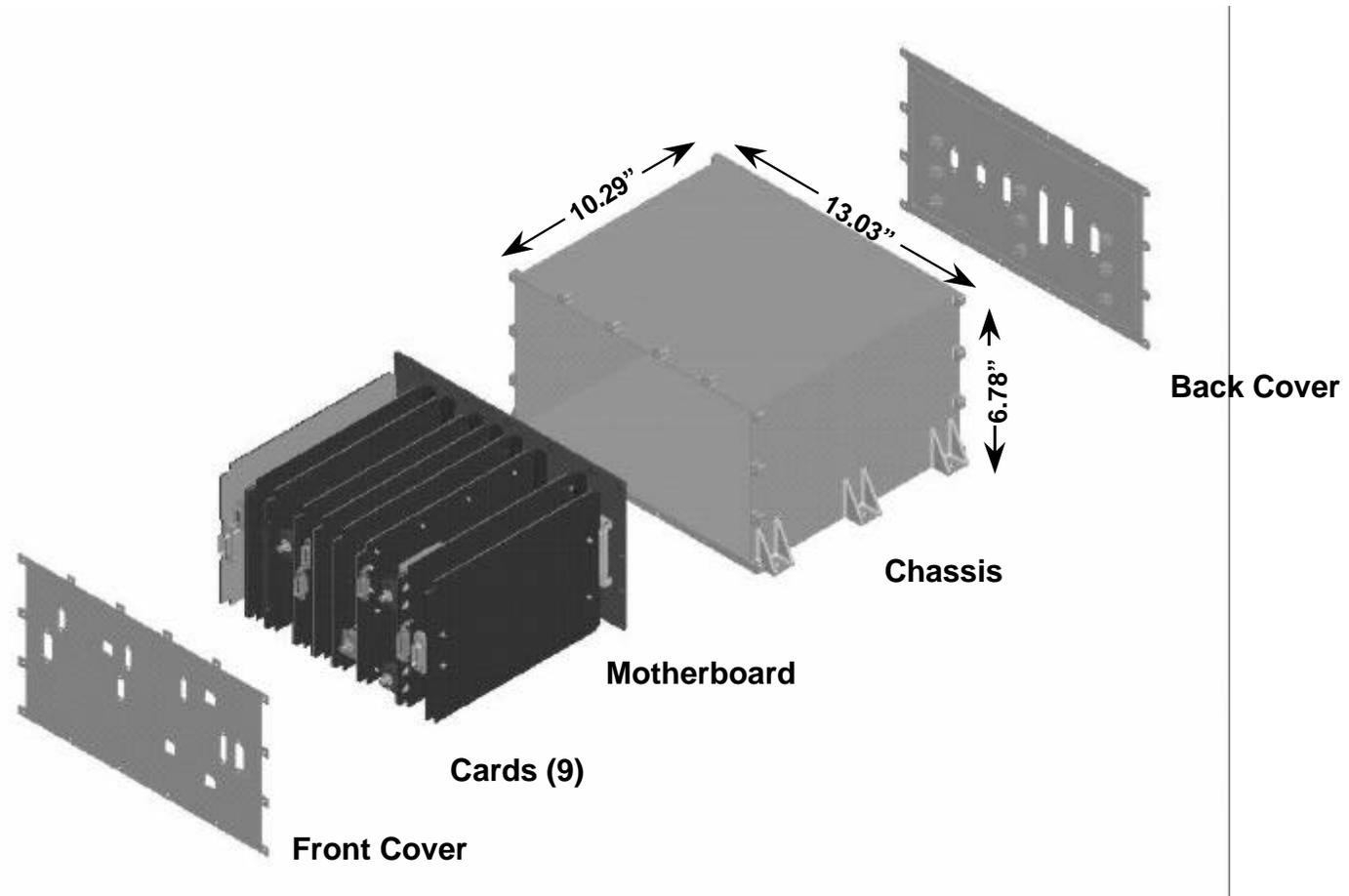


Integrated Electronics Module (IEM)

Configuration Baseline



TIMED IEM CHASSIS



C&DH Hardware Requirements (1 of 3)

- C&DH Processor
 - CPU: 32-bit architecture with 3 VAX-MIPS throughput
 - Memory: 2Mbytes SRAM, 4Mbytes Flash EEPROM
 - I/O: MIL-STD-1553, PCI local bus
- Solid State Recorder
 - 5 to 8 Gbit total data capacity
 - Peak Write Rate: 450kbits/sec
 - Peak Read Rate: 750kbits/sec
 - Simultaneous read & write Operation
 - Random read & write operation
 - Map around bad memory

C&DH Hardware Requirements (2 of 3)

- **Command & Telemetry Subsystem**
 - Route uplink commands from the Critical Command Decoder to the C&DH processor and C&DH processor relay commands to the Critical Command Decoder
 - Collect S/C temperature data and IEM temp and voltage telemetry data
 - Provide interfaces for high rate instrument science data
 - Receive CCSDS telemetry packets from C&DH Processor and parses them into RS-code blocks for SSR storage
- **Downlink Framer**
 - Produces realtime, recorder and null telemetry frames based upon buffered data collected and stored in local RAM and provides a serial data stream to the RF modulator.
 - Timing chain to provide UT and 1Hz time marking (based upon S/C oscillator clock)

C&DH Hardware Requirements (3 of 3)

- Uplink Critical Command Decoder
 - Receive CCSDS compatible commands from the Uplink Receiver command detector (or from the GSE).
 - Route all commands to the C&DH processor, via the C&T subsystem.
 - Route all relay commands, either uplinked or generated by the C&DH processor, to the power switching subsystem.
 - Perform autonomous load reduction upon receipt of a low bus voltage indication from the power subsystem (execute a stored set of relay commands for orderly load reduction).

Subsystem Implementation Drivers (1 of 2)

- C&DH Processor
 - Use TIMED C&DH Processor: Mongoose-V, @12Mhz, 2MByte SRAM, 4MByte EEPROM, 1MByte console boot ROM, 1553 bus, PCI bus.
 - May need to identify and incorporate alternative SRAM and EEPROM components (parts used on TIMED may no longer be available)
 - Board layout modifications required to accommodate new and/or increased memory requirements.
- Command & Telemetry Subsystem
 - Decision of RIU vs. RIO vs. Local I/O temperature collection and conversion will impact board design.
 - Addition of RS-422 data link
 - Any new system interfaces will be added to this subsystem; May force the requirement of an additional card.

Subsystem Implementation Drivers (2 of 2)

- Solid State Recorder
 - Make vs. Buy trade study is required. Primary emphasis on maximizing data capacity for minimum cost, given 2002 launch.
- Downlink Framer
 - System SSR configuration affects the design
 - Internal SSR: A multiple SSR card design will affect the internal data handling scheme for data retrieval from the SSRs. This would be an FPGA design change. May require the addition of another FPGA & most likely affect the board layout.
 - External SSR: Redesign required. Most obvious result is a change as to how data is passed from the SSR, through the C&DH processor and on to the Framer.
 - Timing changes will require FPGA redesign due to different downlink rates.

Candidate Trade Studies (1 of 3)

- Solid-State Recorder - Make vs. Buy
 - “Buy” Considerations:
 - Look for Off-the-Shelf design that can be interfaced to the IEM. If not MIL-STD-1553, will require special (additional) interface on the IEM side.
 - Specify custom-IEM PCI interface. Will require vendor engineering.
 - “Make” Considerations:
 - Duplicate existing IEM SSR design using multiple copies.
 - Redesign SSR taking advantage of denser memory technology, perhaps requiring only a single card.

Candidate Trade Studies (2 of 3)

- RIU vs. RIO vs. Local I/O
 - Remote Interface Unit Considerations
 - Existing TIMED design. Minor C&T Subsystem FPGA changes required to accommodate different number of units .(I²C Interface)
 - Remote I/O Chip Considerations
 - Further “Advanced Technology Development” required in the areas of device characterization, qualification and packaging.
 - Minor C&T Subsystem FPGA changes required to accommodate design differences in the I²C Interface.
 - Local I/O Conversion Considerations
 - Significant C&T Subsystem board level changes. Requires addition of temperature sensor A/D channels and connector.
 - Elimination of I²C Interface.
 - Mass: trade of remote interface units vs. harnessing & connectors

Candidate Trade Studies (3 of 3)

- Enhanced Processor Design for consolidation of C&DH processor functions and Attitude Flight Computer functions.
 - 20-Mhz Mongoose processor design
 - Feasibility study required to determine if there sufficient processing power is available to accomplish both C&DH and G&C functions
 - Significant potential savings in terms of hardware development costs by eliminating AFC as a separate design.

Component Status Summary

COMPONENT	MAKE/BUY	COMMENTS
C&DH Processor	MAKE STUDY	Modify TIMED board layout for new memory components. Study processor speed enhancement.
C&T Subsystem	MAKE	Modify TIMED board design. Addition of RS-422 and possibly housekeeping tlm channels.
Solid-State Recorder	STUDY	Options: Replicate TIMED design, upgrade TIMED design, purchase new design.
Critical Command Decoder	MAKE	Modify TIMED Design: Field-Programmable Gate Array residing on the RF Uplink Card.
Downlink Framer	MAKE	Modify TIMED Design: 2 Field-Programmable Gate Arrays residing on the RF Downlink Card.
IEM Motherboard	MAKE	New board design.
Remote (Temp) Interface Units	STUDY	TIMED RIU vs. RIO Chip Implementation vs. Centralized collection & conversion.

Component Mass Summary

COMPONENT	MASS* (kg)	COMMENTS
IEM		
C&DH Processor	0.51	* All mass numbers are measured TIMED values. Slight variation should be expected with new board designs.
C&T Subsystem	0.44	
Solid-State Recorder	0.55	
Downlink Subsystem	0.55	
Uplink Subsystem	0.75	
IEM Motherboard	0.84	
DC/DC Converter Card #1	0.91	
DC/DC Converter Card #2	0.95	
Housing w/covers	3.45	
Total IEM Mass	10.5	Excluding RIUs. Expected to be comparable to TIMED IEM, stated below.
Remote (Temp) Interface Units	0.23	Mass per unit.
MISC.		
REFERENCE: TIMED Integrated Electronics Module (IEM)	10.5	Mass: Engineering Model, uncoated boards, includes populated RF cards & 2 DC/DC converter cards.

Component Power Summary

COMPONENT	POWER (W)	COMMENTS
IEM		
C&DH Processor	10.4	
C&T Subsystem	2.7	
Solid-State Recorder	5.5	Power for each subsystem. Assume 3 used in IEM.
Downlink Subsystem	3.6	Power reflects digital electronics only (i.e. no transmitter)
Uplink Subsystem	6.5	
IEM Motherboard	N/A	
Remote (Temp) Interface Units	0.3	Power reflects TIMED RIU, per unit. Assume 5 used on S/C.
Peak Converter. Output Power	42	Assumes 3 SSRs and 5 RIUs.
Peak IEM Power	60	@ 28V, assumes 70% converter efficiency
Average IEM Power	54	@ 28V, based upon TIMED IEM Engr. Model measurements
MISC.		
REFERENCE: TIMED Integrated Electronics Module (IEM)	65 (Ave.)	Power: @28V, nominal conditions. Peak worst case design value = 73 W