

STEREO

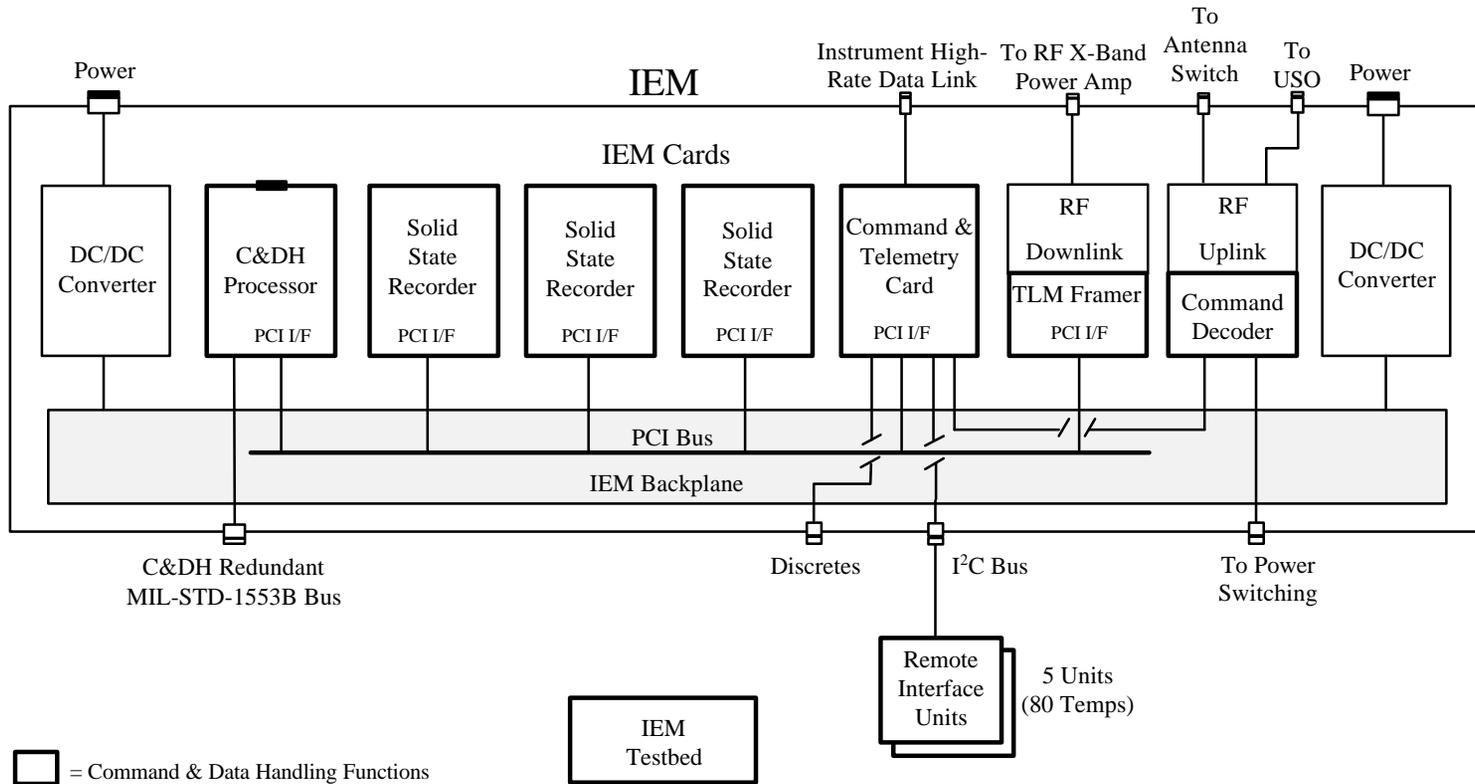
Command & Data Handling Integrated Electronics Module Subsystem Overview [Migrating TIMED to STEREO]

Dan Rodriguez

Ext. 8619

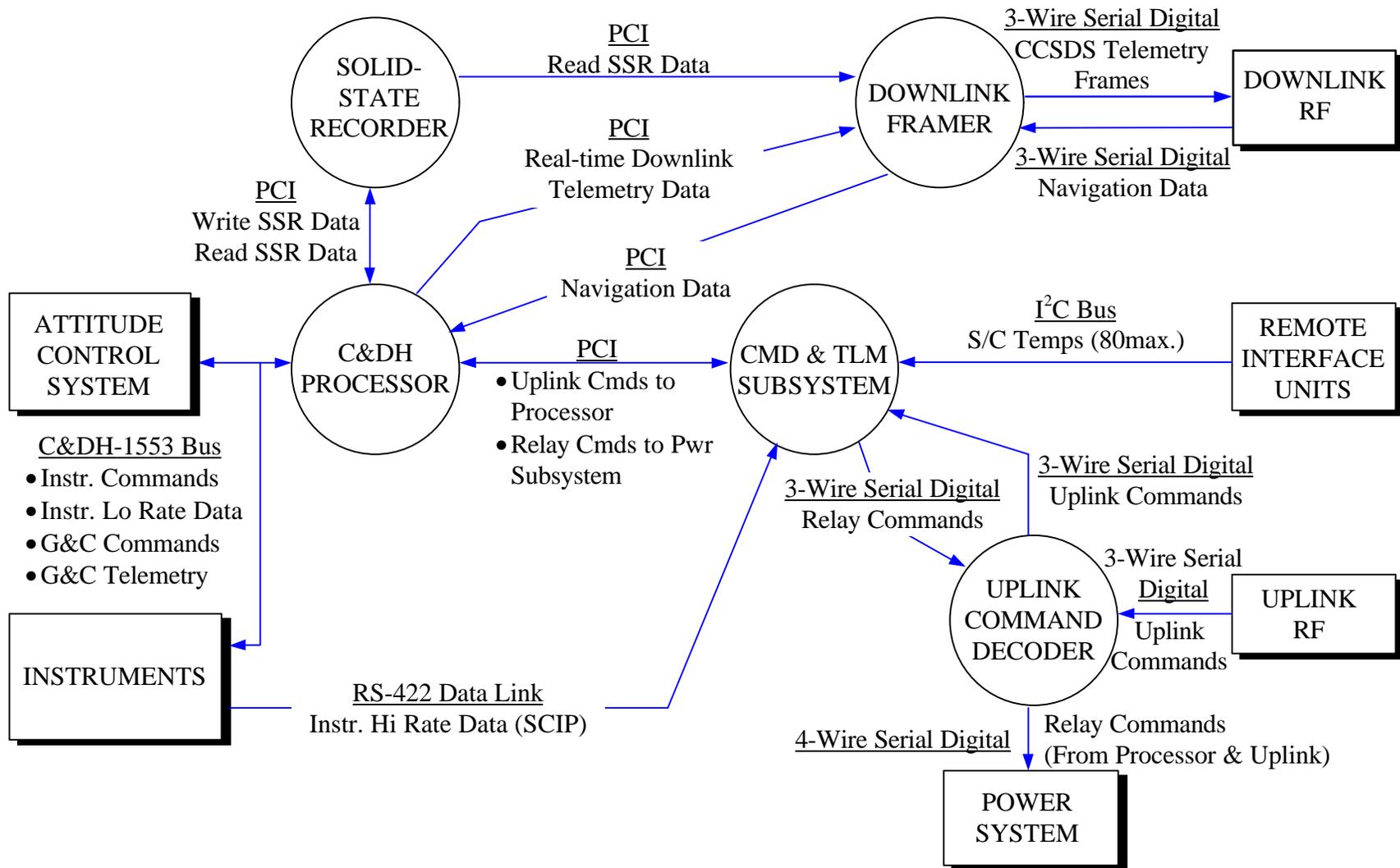
4/8/99

C&DH INTEGRATED ELECTRONICS MODULE SUBSYSTEM FUNCTIONAL PARTITIONING

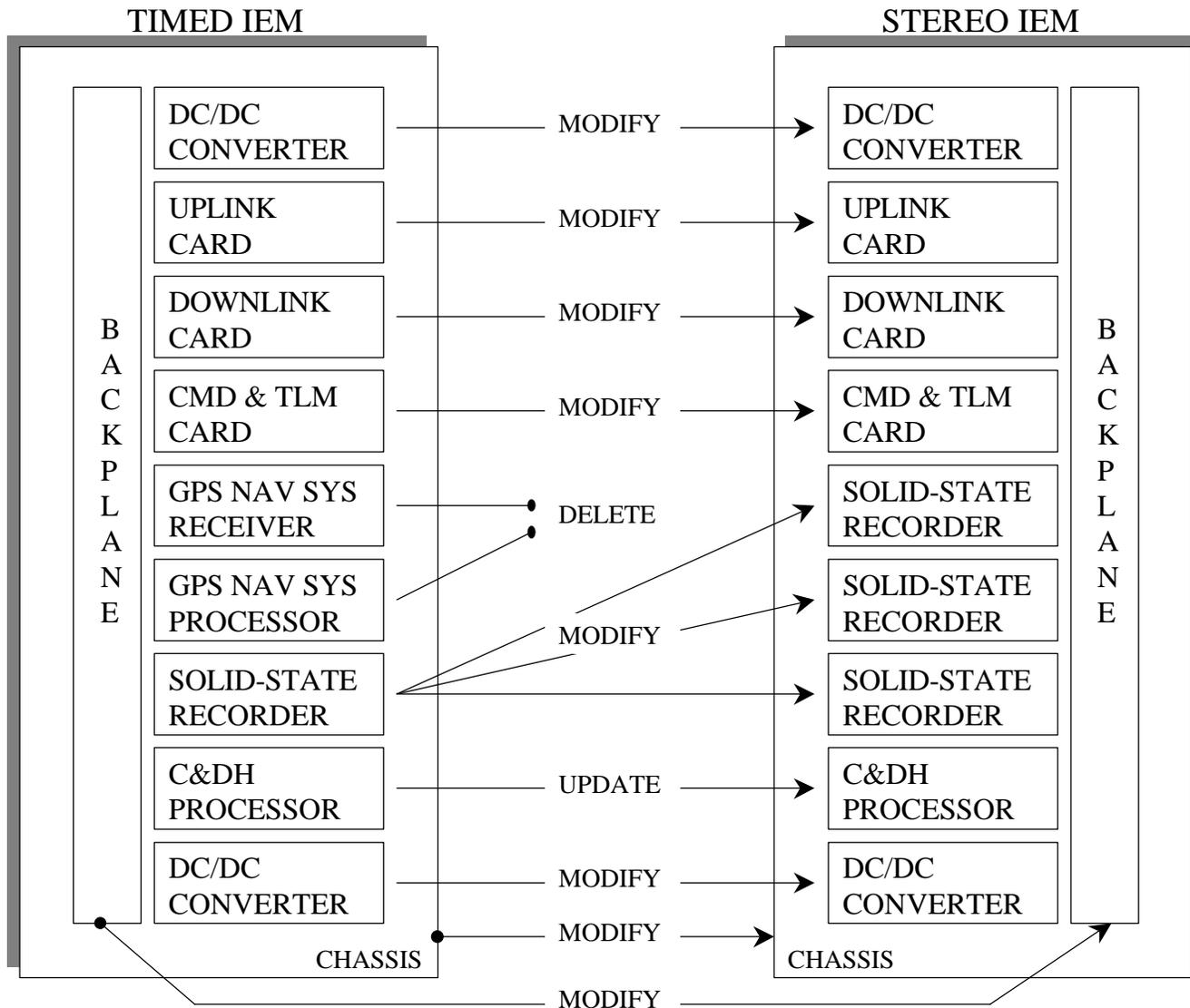


C&DH INTEGRATED ELECTRONICS MODULE

SUBSYSTEM DATA INTERFACES



C&DH INTEGRATED ELECTRONICS MODULE ***MIGRATING FROM TIMED TO STEREO*** (1 of 5)



C&DH INTEGRATED ELECTRONICS MODULE

***MIGRATING FROM TIMED TO STEREO* (2 of 5)**

<i>IEM SUBSYSTEM</i>	<i>TASK</i>	<i>ISSUES & COMMENTS</i>
C&DH PROCESSOR	<ol style="list-style-type: none"> 1. Retain TIMED design. 2. Substitute new devices for SRAM and EEPROM memory in the current design that is no longer available. 3. Board layout changes will be required to accommodate new memory device footprints. 	<ol style="list-style-type: none"> 1. Potential for shared STEREO/ CONTOUR engineering & drafting efforts to accommodate new memory. 2. STEREO should consider participation in a shared parts purchase effort to conserve cost for Mongoose V, memories and 1553 components.
SOLID- STATE RECORDER	<ol style="list-style-type: none"> 1. Retain existing 2.5 Gbit TIMED design <ul style="list-style-type: none"> - Minor FPGA re-design and board layout modification to accommodate unique PCI bus addressing. 2. Three card copies are required, per spacecraft. 	<ol style="list-style-type: none"> 1. Funding for memory (64Mb DRAMS) radiation screening needs to be made available as soon as possible to identify usable part lots. 2. Significant functional & performance test time is involved for each SSR card. 3. An upgraded design may be sought by CONTOUR aimed to enhance performance and allow for increased capacity (~10Gbit/card). STEREO may be able to benefit from this endeavor.

C&DH INTEGRATED ELECTRONICS MODULE

***MIGRATING FROM TIMED TO STEREO* (3 of 5)**

<i>IEM SUBSYSTEM</i>	<i>TASK</i>	<i>ISSUES & COMMENTS</i>
COMMAND & TELEMETRY CARD	<ol style="list-style-type: none"> 1. Moderate re-design and addition to TIMED implementation. 2. Add 400Kb/s RS-422 interface for SCIP 3. Modify on-board A/D signal conditioning channels to accommodate IEM housekeeping telemetry changes. 4. Retain TIMED Remote Interface Unit (RIU) external temperature monitoring system. 	<ol style="list-style-type: none"> 1. Approximately one-third of the existing TIMED card is available for the addition of the RS-422 interface (plenty of room). 2. Interface protocols for instruments using RS-422 links will not be known until instrument identification and selection is complete and/or a determination is made whether or not to use an external DPU.
DOWNLINK (C&DH/ Telemetry Framer)	<ol style="list-style-type: none"> 1. Modify TIMED design to accommodate new downlink rates. 2. Modify TIMED design to accommodate Non-Coherent Navigation function. 3. Add clock divider for 1Hz timing signal (1PPS) 4. Add Mission Elapsed Time (MET) counter 	<p>The CONTOUR program is pursuing a new RF and digital board design and is being influenced to accommodate requirements for both programs. This would yield a design also capable of satisfying the STEREO mission and save cost.</p>

C&DH INTEGRATED ELECTRONICS MODULE

***MIGRATING FROM TIMED TO STEREO* (4 of 5)**

<i>IEM SUBSYSTEM</i>	<i>TASK</i>	<i>ISSUES & COMMENTS</i>
UPLINK (C&DH/Command Decoder)	<ol style="list-style-type: none"> 1. The TIMED functional and board design will remain largely intact. <ol style="list-style-type: none"> a. Retain TIMED CCSDS uplink command handling and relay decoding implementation (One command per CLTU. Up to 128 relay commands and 16 discrete commands accommodated) b. Retain power system interface for relay command transfer. 2. Field-Programmable Gate Array (FPGA) re-design required to accommodate “Hard LVS” stored command sequence, if implemented. 	The digital board design is expected to remain the same as was used on TIMED. Design changes are contained within FPGA devices.
DC/DC CONVERTER	<ol style="list-style-type: none"> 1. Modify TIMED designs. <ol style="list-style-type: none"> a. Changes needed to power additional SSR cards (increased 3.3V loading) b. RF transmitter DC power requirement removed from IEM. 	<ol style="list-style-type: none"> 1. Two separate converter cards are used in the TIMED implementation. 2. A 3.3V converter may be required in lieu of linear regulator in current design.

C&DH INTEGRATED ELECTRONICS MODULE
MIGRATING FROM TIMED TO STEREO (5 of 5)

<i>IEM SUBSYSTEM</i>	<i>TASK</i>	<i>ISSUES & COMMENTS</i>
MOTHER-BOARD	<ol style="list-style-type: none"> 1. Modify TIMED printed circuit backplane. <ol style="list-style-type: none"> a. Modifications required to accommodate additional SSR cards. b. Modifications required to accommodate connector-to-backplane re-assignment, additions and deletions. 	Significant printed circuit track routing adjustments are required to incorporate multiple SSR cards and to eliminate the TIMED GPS Navigation System cards.
CHASSIS	<ol style="list-style-type: none"> 1. Retain TIMED 9-card system 2. Design and manufacture new front and rear covers to accommodate mission specific connector requirements. 	
REMOTE INTERFACE UNITS (RIU)	<ol style="list-style-type: none"> 1. Replicate exact TIMED design. 2. Five copies needed per S/C. 	Build-to-print.

C&DH SYSTEM STATUS SUMMARY

- Recognized need to buy parts for heritage builds as soon as possible to reduce risk of obsolescence resulting in non-availability
- Need to identify and test commercial DRAM lots for total dose and SEU
 - TIMED uses Samsung 64-Mbit EDO DRAMs (40 per card)
 - SOR can purchase parts but radiation testing must be funded
- Instrument interface protocols cannot be defined until instruments are identified
- Non-coherent Doppler navigation issues continue to be addressed
 - Counters will now reside in the downlink subsystem (moved from uplink subsystem in TIMED).
 - Allows the navigation data to be either placed directly into the frame subheader or read by the C&DH processor via the PCI bus and formatted into navigation packets.
- Continue to monitor CONTOUR mission development to identify areas of hardware commonality