APPENDIX C

Data Processing Unit Conceptual Design

A conceptual design for an instrument Data Processing Unit (DPU) was completed as part of the STEREO Pre-Phase A study. Although the current spacecraft baseline does not include a DPU, a design has been developed for use should there be instruments proposed that could benefit from one. A DPU would be beneficial in two cases. In the first case, the proposed instrument is an existing design that is incompatible with the STEREO spacecraft bus. A DPU would be used to adapt the instrument to the STEREO spacecraft and minimize instrument redesign costs. In the second case, the proposed instrument is a new design with modest data processing requirements. A DPU would be shared among multiple instruments to reduce total spacecraft cost.

The DPU would act as an interface unit between the instruments and the fixed interfaces of the STEREO spacecraft. Four of the instruments defined in the STEREO Instrument Announcement of Opportunity (AO) are considered candidates for utilizing an instrument DPU. These are the Magnetometer, Radio Burst Tracker, Energetic Particle Detector and the Solar Wind Plasma Analyzer. These instruments have relatively low data bandwidths and data processing requirements making them suitable candidates for sharing a common DPU.

The interfaces between the DPU and the STEREO spacecraft are limited to one primary power circuit at a nominal +28 VDC and a MIL-STD-1553 data bus for commands, telemetry and time distribution. The interfaces between the DPU and the instruments will be defined only after final instrument selections have been made. For the purposes of this study, it has been assumed that the instruments receive formatted digital commands and output formatted digital telemetry. A science data path consisting of analog signals between an instrument and the DPU could be accommodated but is not recommended due to integration, calibration and noise issues.

The primary task of the DPU would be to reformat instrument commands and telemetry for compatibility with the STEREO spacecraft MIL-STD-1553 data bus. In addition, the DPU would provide data processing and data compression services (if necessary) to the instruments as DPU processing capability and bandwidth permit. The DPU would also time tag instrument data as required and accommodate a limited amount of voltage, current and temperature monitoring for the instruments.

The design of the STEREO Instrument DPU is a second-generation design based upon the instrument DPU designed for the Near Earth Asteroid Rendezous (NEAR) spacecraft and used on the Advanced Composition Explorer (ACE) and Cassini spacecraft. It is a modular computer system consisting of a core set of boards with custom instrument interface cards added as required. The core set of boards consists of a processor board, a MIL-STD-1553 interface board, a housekeeping voltage, current and temperature monitoring board and a DC/DC converter board. The instrument interface boards would be application specific and would be based upon field programmable gate arrays (FPGAs) with memory components added as needed to buffer instrument data. Second-generation enhancements to these boards include updated memory components, updated FPGAs and stacking inter-board connectors. The stacking inter-board connectors eliminate the system motherboard thereby reducing system size, mass and cost.

The modular nature of the design is enhanced with a modular electronics chassis similar to that used by the APL Command and Data Handling System in Your Palm project. Each four-inch by four inch electronic board, with stacking inter-board connector, is housed in a frame. When stacked and connected with the other electronic boards in the system the boards form the top, bottom, front

and back walls of the electronic chassis. End plates are added and the entire assembly is through-bolted together to form a completed unit. This approach minimizes chassis design costs because only three piece parts need be designed: the 0.50 inch thick board frame used by most boards, the 0.75 inch thick board frame used by the DC/DC converter boards and the endplate. A system with any number of boards can be built from these piece parts. The board frames will be modified by machining openings for right angle micro-miniature "D" connectors as required for each board.

A block diagram of the DPU is shown in Figure C-1. Power and mass figures are given in Table C-1. The DPU consists of the four core boards and two application specific instrument interface boards. The processor board is based upon the 16 bit RTX2010RH processor operating at 6 million instructions per second (MIPS). It contains 64 Kbytes of Programmable Read Only Memory (PROM), 256 Kbytes of Electrically Erasable Programmable Read-Only Memory (EEPROM), 256 Kbytes of Static Random Access Memory (SRAM), an FPGA for processor support and interface functions and a customizable external interface connector. The MIL-STD-1553 interface board is based upon the United Technologies Microelectronics Center (UTMC) Summit DX protocol processor and data transceiver with an FPGA for interface functions and 64 Kbytes of buffer SRAM. The DC/DC converter board is based upon hybrid converter and filter modules. It incorporates in-rush current limiting circuitry, under-voltage lockout circuitry and output noise filtering. The housekeeping voltage, current and temperature monitoring board uses input multiplexers and signal conditioning operational amplifiers to feed a single analog to digital converter (ADC). An FPGA is used to control data acquisition and interfaces the system to the processor.

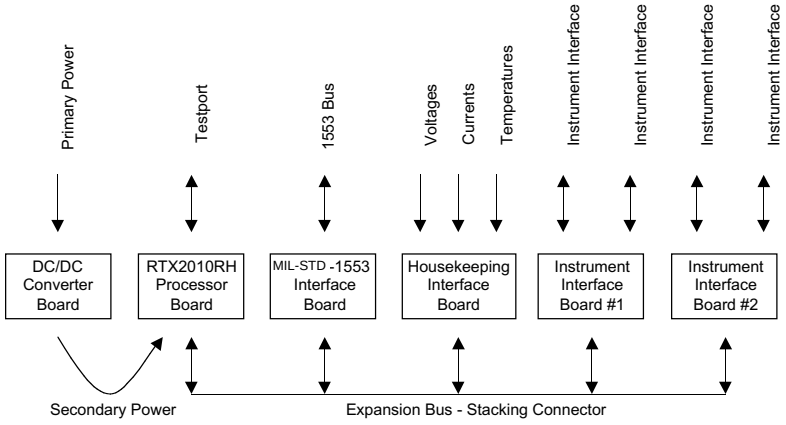

Figure C-1 DPU Block Diagram

Table C-1 DPU Power and Mass

Unit	Board Weight (grams)	Chassis Weight (grams)	Power (watts)	Thickness (inches)
Processor Board	125	25	1.00	0.50
MIL-STD-1533 Board	125	25	0.50	0.50
Housk eeping Boar d	125	25	0.50	0.50
DC/DC Con ver ter Boar d	175	55	1.50	0.75
Instr ument Interf ace Board	125	25	1.00	0.50
Instr ument Interf ace Board	125	25	1.00	0.50
Chassis End Plate	0	60	0.00	0.06
Chassis End Plate	0	60	0.00	0.06
Total	800	300	5.50	3.37

Estimated Power: **5.50 watts**
Estimated Weight: **1.10 kg**
Estimated Dimensions: **4.2 x 4.2 x 3.4 inches** (not including mounting feet)

Three of the four core boards in the system are based upon existing designs. The processor board is very similar in design to the processor board used in the instrument DPUs that were flown on the NEAR, ACE and Cassini spacecraft. The updated memory components for this processor board are used in the High Energy Neutral Atom (HENA) instrument DPU currently qualified and awaiting launch. The MIL-STD-1553 interface board is similar in design to the interface board used on the NEAR spacecraft and would be software compatible with the existing unit. The DC/DC converter board uses the same components and circuit design as used in the HENA and GUVI instruments. The change in connectors and board size necessitates a new board layout. The housekeeping board would be a new design and could be tailored to the requirements of the selected instruments. Circuit design of this board would be based upon similar boards developed for NEAR, Cassini and HENA.

Area studies of the processor board, MIL-STD-1553 interface board, and the DC/DC converter board were completed to verify the feasibility of packaging these functions onto the four inch square board form-factor. A detailed printed circuit board routability study of the processor board was completed to insure that the parts packing assumptions used in the area studies were valid. Both studies indicated that the system is feasible and would not present packaging problems.